## ABSTRACT

There is disclosed herein a multi-port frequency step-down queue that efficiently transfers data from a fast clock domain to a slow-clock domain having parallel hardware resources. In one embodiment, the queue includes a set of registers that are sequentially selected by an input counter that receives the fast clock. As the registers are selected, they store a data item from the input data stream. The queue also includes multiple multiplexers each having inputs that are sequentially selected by an output counter that receives the slow clock. The first multiplexer is coupled to the first N registers in the queue, the second multiplexer is coupled to the second N registers in the queue, etc. In this manner, the step-down queue generates multiple output FIFO data streams at the slower clock rate. Each of the output data streams may then be processed in parallel.